UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,062,591 B2
APPLICATION NO. : 09/967126
DATED : September 28, 2001
INVENTOR(S) : Victor Key Pecone

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 15, line 41, cancel the text beginning with "11. A method for sharing data" to and ending "memory modules." In column 15, line 56 and insert the following claim:

11. A method for sharing data between a first controller memory module and a second controller memory module, comprising:

providing a first shared path in a first channel interface module (CIM), wherein the shared path includes a switchable component for determining which data is to be routed over the shared path;

wherein the first shared path is included on a data path between the first and second controller memory modules;

a direct memory access engine for each of said first and second controller memory modules; and

transferring first data between said first controller memory module and said second controller memory module using said direct memory access engine for at least one of the first and second controller memory modules, wherein said switchable component provides passage of said first data over said first shared path between the first and second controller memory modules.

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Column 15, line 57, cancel the text beginning with "12. The method of claim 11, further comprising:" to and ending "shared path." In column 15, line 64 and insert the following claim:

12. The method of Claim 11, further comprising:

providing a second shared path in a second channel interface module;

wherein the second shared path is included on a data path between the first and second controller memory modules, and the second shared path includes a second switchable component for determining which data is to be routed over the second shared path; and

transferring second data between said first controller memory module and said second controller memory module using said direct memory access engine in the first controller memory module and another direct memory access engine in the second controller memory module, wherein the second data passes through said second shared path.

Column 15, line 65, cancel the text beginning with "11. The method of claim 11, further comprising:" to and ending "of transferring." In column 16, line 3 and insert the following claim:

13. The method of Claim 11, further comprising:

connecting said first channel interface module to both said first and second controller memory modules via a passive backplane, wherein the first data passes through the passive backplane during said step of transferring.

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Column 16, line 4, cancel the text beginning with "14. An apparatus for sharing data" to and ending "shared path." In column 16, line 22 and insert the following claim:

14. An apparatus for sharing data between a first controller memory module and a second controller memory module, wherein each of the first and second controller memory modules is for controlling communication of storage data between one or more host computers and one or more storage devices, comprising:

at least a first channel interface module having a first shared path, wherein the shared path has a switchable component, operably associated therewith, for selecting which data is to be routed on the shared path;

a first controller memory module including a first direct memory access engine;

a second controller memory module including a second direct memory access engine;

wherein the first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage devices, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device;

a communications interface to permit direct communications between said first and second controller memory modules; wherein data is transferred between said first and second controller memory modules using at least one of said first and second direct memory access engines, and using the switchable component, and wherein the direct communications are not routed through the first host computer.

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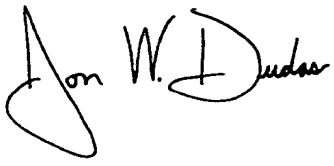
Claim 20, line 2 "clannel" should read --channel--.

Signed and Sealed this

Twenty-sixth Day of September, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office